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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/460,742	12/14/1999	RAJENDRAN NAIR	884.229US1	2896

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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER
TRA, ANH QUAN

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 11/20/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

P5

Office Action Summary	Application No.	Applicant(s)	
	09/460,742	NAIR ET AL.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-6,9,10 and 14-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4-6,9,10 and 14-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Prosecution Application

1. The request filed on 09/30/2002 for a Continued Prosecution Application (CPA) under 37 CFR 1.53(d) based on parent Application No. 09/460742 is acceptable and a CPA has been established. An action on the CPA follows. A new ground of rejection is introduced.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 4, 14 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Manning et al. (USP 5962887).

As to claim 4, Manning teaches in figures 1 and 2, and column 1, line 59 to column 2, line 19, a circuit comprising: a voltage node (node that providing voltage 160, column 2, line 8); a ground node (node that providing ground potential, column 2, line 10); and a transistor (figure

1) including a gate (100), a drain (130 or 140), and a source (140 or 130), the gate being coupled to the voltage node (column 2, line 8) and the drain and source being coupled to the ground node (column 2, lines 9 and 10, figure 8 further shows the bottom plate of transistor capacitor comprises drain and source coupled together), the transistor operating in the depletion mode (depending on the value of voltage 160, figure 2 shows transistor 2 is operating in depletion mode for certain of range), the gate comprising a p-type polysilicon (column 1, lines 52-58), wherein the transistor has a variable capacitance characteristic (figure 2) that is capable of decreasing noise signals above an absolute value of an operating voltage value at the voltage node and increasing noise signal below the absolute value of the operating voltage value.

As to claim 14, figures 1 and 2 show a circuit comprising a die; a ground node (node that providing ground voltage, column 2, line 10) located on the die; power supply voltage node (node that providing voltage 160, column 2, line 8); and an electronic device (figure 1) having a variable capacitance characteristic (figure 2) and that is permanently coupled between the ground node and the power supply voltage node and capable of providing an asymmetrical response to incremental voltage variations about an operational node voltage at the power supply voltage node.

As to claim 15, since electric property of the capacitor as shown in figure 1 and 2 is the same as the claimed capacitor transistor whose property is shown in figure 1B of the application and the prior art discloses all the claimed structure, the accompanying characteristics including the damping and amplifying are also inherent.

4. Claims 9 and 10 rejected under 35 U.S.C. 102(b) as being anticipated by Mead et al. (USP 5844265).

As to claim 9, Mead et al discloses in figure 1 a circuit comprising a die having a high power supply voltage node (18) and low power supply voltage node (28); and a transistor (32) coupled between the high power supply voltage node and the low power supply voltage node and operable for controlling a voltage at the low power supply voltage node.

As to claim 10, figure 1 shows the transistor has a gate, a drain, and a source, and the gate is coupled to the high power supply voltage node and the source and drain are coupled to the low power supply voltage node.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 5, 6, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Manning et al. (USP 5962887).

As to claims 5 and 16, Manning et al.'s figures 1-2 and columns 1-2 teach all limitations of the claim except for the operating voltage between about 0.5 volts and about 1.5 volts or at 1.3 volts. However, the selection of the operation voltage to be between about 0.5 volts and bout 1.5 volts or at 1.3 volts is seen as an obvious design expedient dependent upon particular environment of use to ensure optimum performance.

As to claim 6, figures 1-2 shows all limitations of the claim except for a logic cell coupled to the voltage node and close to the transistor. However, it is seen as an obvious design choice for using the supply voltage (160) as a supply voltage for any logic cell and fabricate the

logic cell close to the transistor dependent upon particular environment of use to ensure optimum performance.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 703-308-6174. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

QT
November 5, 2002

Terry D. Cunningham
Primary Examiner